# Introduction to Electronic Hardware – Assessment 2
# Fuel level indicator

*To be handed in to the Electronics Departmental office by:*
*12 noon, 17th January 2011 (Monday, Week 2)*

## 1 Introduction

This document describes the second assessment for the Stage 1 module Introduction to Electronic Hardware (0780221). It describes the scope of the assessment and how it will be marked. It also provides some references to material on report writing and guidance on how to approach the assessment, including acceptable practice.

## 2 Scope of the assessment

In this assessment you are expected to use the information on op-amps and digital circuits that you have gained during the lecture course and to combine it with new information that you will have to find out by reading books from the library and sources on the internet. You may have to apply some principles of circuit design that you have not seen before.

### *2.1 The design requirement*

A sensor for monitoring the amount of fuel in a tank outputs a voltage, $v_{fuel}$, in the range 0 V (tank completely empty) to 3 V (tank completely full). Your manager has asked you to prototype a digital display to show how much fuel is left in the tank. He wants you to use a digital ramp analogue-to-digital converter (ADC) and has begun the design for you. The amount of fuel left is to be displayed using a single 7-segment display digit. The display is required to show the letter 'E' when the tank is empty or almost empty and the letter 'F' when the tank is full or nearly full. For increasing levels of fuel between these two extremes the display should show the digits 1 to 9.

### *2.2 The Research*

Research the digital ramp analogue-to-digital ADC so that you understand its principle of operation.

Figure 1 shows one method for implementing a digital ramp ADC (note: this may not be exactly the same as the circuits you have researched). The resistances of resistors R1 to R4 are related such that R3 = 2 x (R4), R2 = 2 x (R3) and R1 = 2 x (R2). You may assume that the digital components (CTR1, REG1, DEC1 and the inverter) are HCT logic family devices [2]. OA1 to OA3 are devices inside a TL074 quad op-amp package [3]. The power supply voltages are $V_P$ = 5 V and $V_M$ = -5V.

Describe in no more than one page the operation of the digital ramp ADC in Figure 1. Consider each stage in turn and how they combine to perform the overall function.

### *2.3 The Design*

a) Calculate suitable resistances for R1 to R5 so that the binary values from the counter produce voltages from 0 V to approximately 3.75 V in approximately 0.25 V steps at point **K** in the circuit.

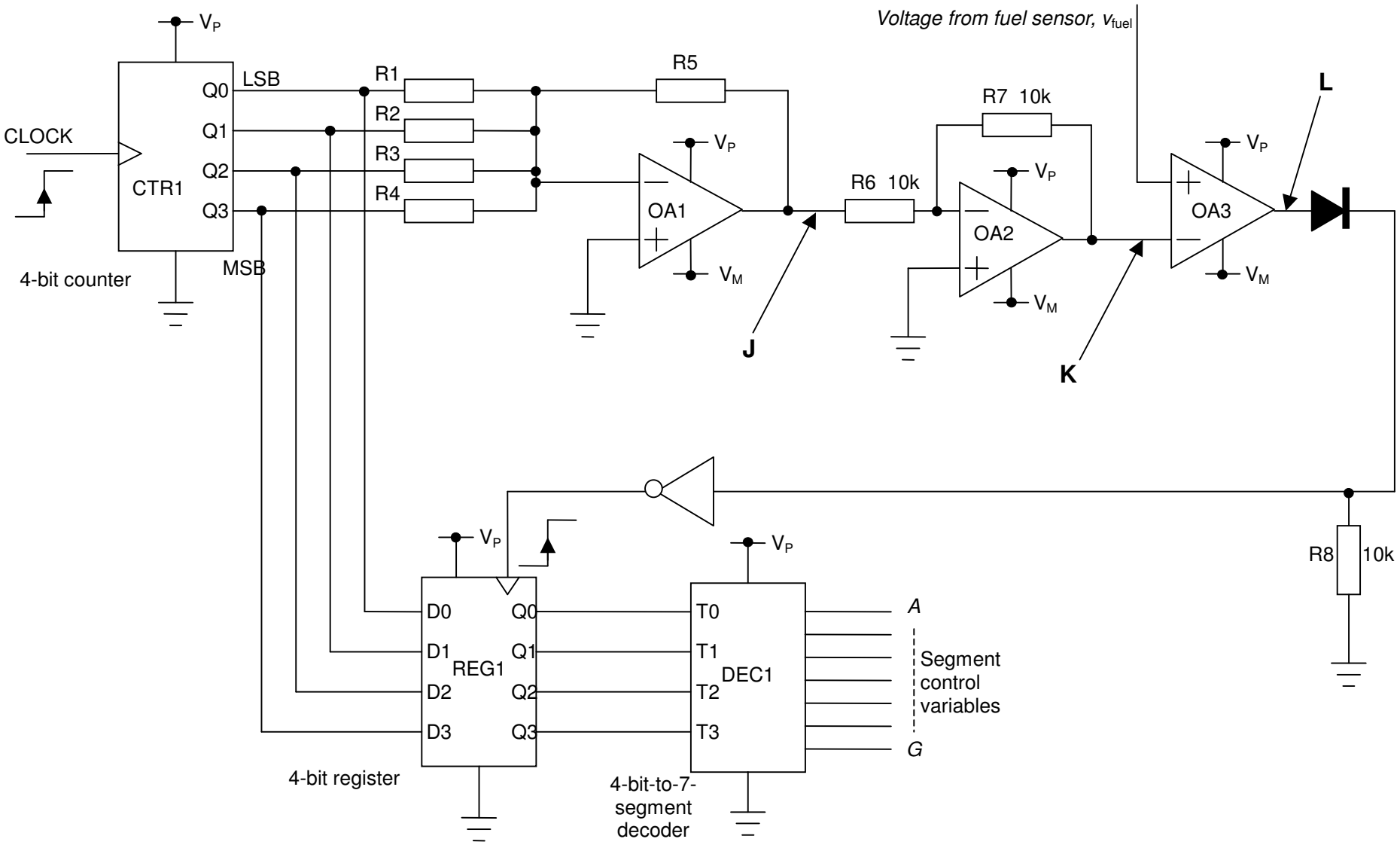



Figure 1

b) Draw on the same axes a graph of the waveforms at points **J** and **K** over one complete cycle of the counter CTR1, based on the resistances you calculated in part (a).

c) On the same graph that you drew in part (b) draw the waveform at point **L** when $v_{fuel}$ is 1.6 V.

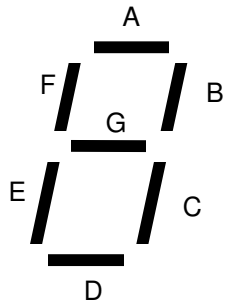
d) The waveform at point **L** is level shifted and inverted and then applied to the clock input of the 4-bit register, REG1. Why is level shifting necessary?

e) What binary value will appear at the outputs Q3 to Q0 of the register REG1, when $v_{fuel}$ is 1.1 V?

| T3 | T2 | T1 | T0 | $V_{FUEL}$ (V) | Active segments |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0.00 | E |
| 0 | 0 | 0 | 1 | 0.25 | E |
| 0 | 0 | 1 | 0 | 0.50 | 1 |
| 0 | 0 | 1 | 1 | 0.75 | 2 |
| 0 | 1 | 0 | 0 | 1.00 | 3 |
| 0 | 1 | 0 | 1 | 1.25 | 4 |
| 0 | 1 | 1 | 0 | 1.50 | 5 |
| 0 | 1 | 1 | 1 | 1.75 | 6 |
| 1 | 0 | 0 | 0 | 2.00 | 7 |
| 1 | 0 | 0 | 1 | 2.25 | 8 |
| 1 | 0 | 1 | 0 | 2.50 | 9 |
| 1 | 0 | 1 | 1 | 2.75 | F |
| 1 | 1 | 0 | 0 | 3.00 | F |
| 1 | 1 | 0 | 1 | 3.25 | F |
| 1 | X | 1 | 0 | 3.50 | |
| 1 | X | 1 | 1 | 3.75 | |

(X = don't care)

(a)




(b)

Table 1: Specification for the 4-bit-to-7-segment decoder

Table 1(a) defines the required 7-segment display patterns for each 4-bit binary number presented to the 4-bit-to-7-segment decoder inputs, T3 to T0. Table 1(b) associates each Boolean variable, A to G, with the segment it controls.

f) When the Boolean variable *A* equals one, segment A is active; when *A* is zero, the segment is inactive. Produce a truth table which shows the four inputs, T3 to T0 and the states of *A* for each binary value.

g) Showing your working, find the minimised sum-of-products expression for controlling segment A. Note any choices you make.

h) Given that the minimised sum of products expression for controlling segment C is $C = \overline{T3}\,T2 + T1\,\overline{T0} + T3\,\overline{T2}\,\overline{T1}$, manipulate this into a form which uses 2-input NAND gates only.

i) What clock frequency would you suggest using?

### *2.4 Recommendations*

In no more than half a page (excluding any diagrams), suggest ways of improving the design, bearing in mind that this is a prototype which might possibly become a commercial product. Do not limit your recommendations to technical details, but try to consider every aspect of the development process.

## 3 The format of your submission

A full report is not required. Answer each point in sections 2.2 to 2.4 using the headings and labels shown and do not include material which is not required.

Your submission should be no more than 4 pages of text in length, including references. No marks will be awarded for any textual content beyond this limit. Diagrams should be placed separately in an appendix and referred to from the text. If typed, the main text should be set in a 12-point font. If handwritten then the text must be neat and legible. Any diagrams should be drawn by the author – not copied directly from references. For word-processed documents you may find it faster to draw diagrams neatly by hand and then scan the diagram using the scanner available in the computer classroom, rather that using computer drawing packages.

## 4 Writing your report

You should refer to the Department of Electronics internal web pages by Chesmore [4] for guidance on report writing or to one of the many books available in the library, such as [1].

## 5 How the report will be assessed

Marks will be awarded as follows:

| Item | Weight | Factors determining mark |
|---|---|---|
| Presentation | 20% | Logical structure, neatness, numbers and titles on figures, correct spelling and satisfactory use of English. |
| Research | 30% | Clarity, succinctness, appropriate use of diagrams. Description of each circuit stage and how they combine. |
| Design | 30% | Systematic presentation which gives confidence in the results. Justifications for decisions and assumptions. |
| Recommendations | 15% | Evidence of reflection and logical thought. Awareness of the various dimensions of the problem. |
| Appropriate use of references | 5% | Evidence of research in written and online material, including and beyond the references supplied, with references in the text indicated using one of the standard methods. |

# 6 Academic misconduct

This is an individual piece of work and you should not collaborate with others in its production. In this work, you are expected to perform your own analysis and write descriptions in your own words. You are expected to draw your own diagrams. Marks will not be awarded for material that is directly copied from other sources.

References should be used to refer the reader to the source(s) of information you have used. Common knowledge items such as the circuit configurations of an op-amp are not normally referenced. If you present information on particular electronic devices, the relevant data sheets should be referenced.

If you copy directly any diagram, words or analysis from another source you should correctly attribute the work. This means stating explicitly that the material was taken from another source. For example, words copied from another source should be indicated as in the following sentence. The Department of Electronics, Undergraduate Handbook, Statement of assessment (2009, Section 3, p17) [5] says:

> "Plagiarism - incorporating within one's work without appropriate acknowledgement material derived from the work (published or unpublished) of another. This includes copying material from the internet."

Plagiarism and any other academic misconduct in submitted reports may result in the penalties described in the Statement of Assessment [5].

# 7 Hand-in and late submission penalty

You should be aware that the University requires a deduction of 10% of the maximum mark (not the actual mark) per day for late submissions of up to 5 days, after which a mark of zero is awarded. If you have extenuating circumstances you should submit an extenuating circumstances form to the departmental office, accompanied by any evidence. Failure of your computer system or loss of data is not considered an extenuating circumstance. Again, you should read the Statement of Assessment [5] for full information. You should not put your name on the report to be marked; **only your examination number** should be used.

## References

1. Horowitz, P. & Hill, W., 1980, The Art of Electronics, Cambridge University Press.
2. HCT logic family specifications
   http://i2c2p.twibright.com/datasheet/HCT_FAMILY_SPECIFICATIONS.pdf
3. TL074 quad op-amp datasheet
   http://www.datasheetcatalog.com/datasheets_pdf/T/L/0/7/TL074.shtml
4. Chesmore, D. Report Writing,
   http://www.amp.york.ac.uk/internal/ugrad/gen/tskills/report_writing/report_1.htm
5. Department of Electronics, 2009, Undergraduate Handbook, Section 3: Statement of Assessment.

   *BEng/MEng:*

   http://www.elec.york.ac.uk/internal_web/ugrad/gen/Yr0_1HBK/3%20Statement%20of%20Assessment%20and%20Progress.pdf

   *BSc:*

   http://www.elec.york.ac.uk/internal_web/bsc/docs/BScYr1Handbook/3%20Statement%20of%20Assessment%20&%20Progress.pdf

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