Loughborough University

ELECTRONICS B

(07ELB010)

JUNE 2008 **3 HOURS**

Attempt **FIVE QUESTIONS** with a **MINIMUM of TWO** from **EACH SECTION**

Each question carries 20 marks

Any university approved calculators are permitted

Charge on an electron = 1.602×10^{-19} C
Boltzmann's constant = 1.381×10^{-23} J/K

SECTION A

1 An OP-AMP having a gain given by $A_d = 2 \times 10^5/(1+jf/7)$ and a slew rate of 1V/μs is used in an inverting amplifier circuit with an input resistance of 100kΩ and a feedback resistance of 1MΩ. The supply voltage is ±15V. Neglecting the OP-AMP input and output resistances:

(a) Determine the small signal bandwidth of the amplifier. [15 marks]

(b) Determine the power bandwidth, stating any assumptions made. [5 marks]

2 (a) Draw the circuit diagram of an OP-AMP integrator having resistor and capacitor values of 1kΩ and 0.1μF respectively. Proving any formula used, determine the output voltage of the integrator if the input is a square wave of 1kHz with amplitude of ±1V. Sketch the input and output voltage waveforms showing all important voltages and times. What would happen if the frequency were to be reduced to 167Hz? Assume the OP-AMP is supplied with ±12V supplies. [12 marks]

(b) Draw the circuit diagram of an OP-AMP differentiator having resistor and capacitor values of 2kΩ and 1nF respectively. Proving any formula used, determine the output voltage of the differentiator if the input is a triangular wave of 100kHz with amplitude of ±5V. Sketch the input and output voltage waveforms showing all important voltages and times. [8 marks]

3 (a) (i) Briefly describe the operation of the 'crystal' in a crystal oscillator. [5 marks]

(ii) Explain how this leads to an oscillator with a good frequency stability. [5 marks]

(b) Explain the meaning of the terms 'thermal (Johnson) noise' and 'shot' noise stating what parameters they depend on. [4 marks]

An amplifier having a voltage gain of 100 has a total noise output voltage of 100μV when driven from a source with 600Ω output resistance. If the effective noise bandwidth is 10kHz and the ambient temperature is 29°C, calculate the noise figure NF in decibels for the amplifier, given that NF is the input signal-to-noise power ratio divided by the output signal-to-noise power ratio. [6 marks]

4. A power amplifier using a **push-pull class-A** output stage is to be designed to deliver a power of 20W into a loudspeaker load of 6Ω.

(a) Give the circuit diagram of the push-pull output stage driving the load [3 marks]

(b) Specify suitable voltage values for the positive and negative supplies and the mean current each must be able to supply, assuming ideal transistors.
Further, specify the quiescent bias current I_{CQ} for the output stage, the maximum collector current $I_{C,max}$, the maximum collector-emitter voltage $V_{CE,max}$ and the maximum power dissipation $P_{C,max}$ for the transistors. [10 marks]

(c) Calculate the required thermal resistance of a heatsink to be attached to the transistors if the heatsink temperature is not to exceed 55°C when the amplifier is operating in a room with an ambient temperature of 35°C.
Further, estimate the maximum junction temperature of the transistors for the above conditions, given that the thermal resistance between the transistor cases and the heatsink is 0.5 °C/W and that the junction-to-case thermal resistance of the transistors is 1.5°C/W. [7 marks]

SECTION B

5 (a) Expand the acronyms FPGA, VHDL and CLB in full. Give a brief explanation of each piece of terminology.

[6 marks]

(b) Describe the distinction between a CLB and a Slice in the context of an FPGA.

[6 marks]

(c) Given the following truth table and logic equation, give a VHDL entity declaration and architecture body for a four input multiplexer with active low enable.

```
Y =   NOT EN      AND ((A AND NOT S1 AND NOT S0)
        OR    (B AND NOT S1 AND S0)
        OR    (C AND S1 AND NOT S0)
        OR    (D AND S1 AND S0))
```

Make use of the following code skeletons

```
entity MUX4TO1 is
...
....
End MUX4TO1;

architecture MYARCH of MUX4TO1 is
begin
...
...
end MYARCH;
```

[8 marks]

/continued

6 a A floating point number format is designed as follows:

MSB	Sign	1 = negative number	0 = positive number
Next 4 bits	Exponent	Biased by 8	
Remaining 11 bits	Fraction	In addition to these 11 bits 1 bit is implied	

Using this format how would the following decimal numbers be represented (MSB leftmost bit)?

35
0.3125
-21.5
-0.0625

[10 marks]

b A microprocessor system is to be designed with a non-volatile program memory that allows the program it contains to be updated at roughly six monthly intervals. Suggest two different semiconductor memory technologies that would be suitable for use in this application with ease of update and cost being significant factors. Compare the two technologies that you have chosen and select just one for implementing the system giving reasons for your choice.

[10 marks]

7 a Most microcontrollers can perform timing operations in either software or by utilizing an 'on-chip' counter timer circuit. Describe how both techniques could be used to generate a pulse at one of the microcontroller's output pins with a fixed duration and identify any advantages or disadvantages associated with each approach..

[12 marks]

b What is the function of the 'Watchdog Timer' that is included in many microcontroller systems?

[4 marks]

c Identify the advantages and disadvantages of designing a digital device such as a microcontroller with an 'open collector' output interface?

[4 Marks]

8 a An 8051 family microcontroller, with a 6MHz clock, is to be used to generate the waveform shown in Figure Q8 on port pin P1.0 which is to be accurately repeated indefinitely once the processor has completed its reset procedures which include setting all ports to output a logic low.

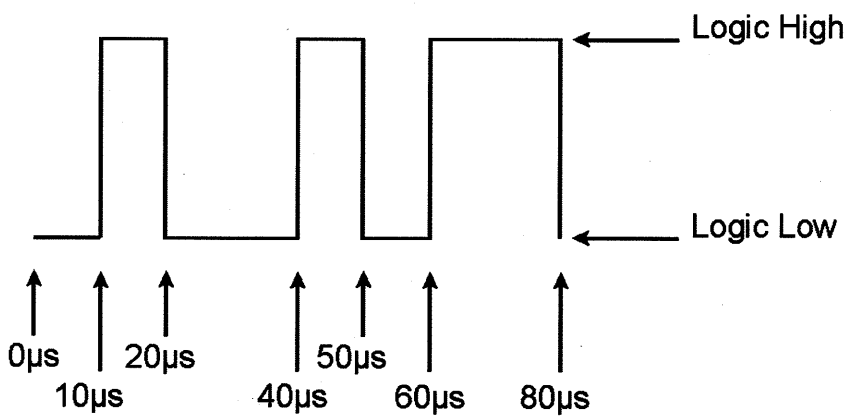

Figure Q8

/continued

Using any combination of the following instruction subset, write a program that will accurately achieve this requirement. Assume that outputs become valid at the end of the instruction that changes the state of a port or its individual pins. Note: 'bytes' indicates the number of bytes that the instruction takes in program memory and 'cycles' indicates the number of machine cycles (there are 12 clocks/machine cycle) that it takes to execute the instruction:

			Bytes	Cycles
ADD	a,#data	Add immediate data to Accumulator	2	1
CLR	A	Clear Accumulator	1	1
CLR	bit	The specified bit is set to zero (eg: CLR P1.0)	2	1
CPL	A	Complement Accumulator	1	1
CPL	C	Complement carry flag	1	1
DJNZ	Rn,rel	Decrement register & jump if not zero	2	2
INC	A	Increment Accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	bit,C	Move carry flag to direct bit	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	Rn,#data	Move immediate data to register	2	1
NOP		No Operation	1	1
SETB	bit	Sets the specified bit to one (eg: SETB P1.0)	2	1
SJMP	rel	Unconditional Jump	2	2

Where:

bit	An internal memory bit, I/O pin, control bit.
#data	An 8-bit constant included in the instruction.
direct	An internal RAM location, I/O port, control or status register.
Rn	One of eight working registers R0 to R7.
rel	Relative address to which a jump is made on appropriate condition.

[16 marks]

b If the reset procedures of the microcontroller enable the external interrupts and interrupt service routines were provided, what would be the effect of an interrupt arriving at one of the two external interrupts 65μs into the waveform sequence?

[4 marks]

C D Manning
W C Gabb
S C Pomeroy

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