DC-Link Capacitor Current Modeling and Analysis for Three-Level Voltage Source Inverters

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***Abstract*—As a critical specification for the dc-link design of a voltage source inverter (VSI), the root-mean-square (RMS) value of the capacitor current should be accurately determined. Various work has been done on the modeling and analysis for the dc-link current, however an accurate model for the dc-link capacitor current still needs to be developed, especially for multilevel inverters. In this work, a detailed model for the dc-link capacitor current of a three-level VSI is proposed, and based on the model, the closed-form expression of dc-link capacitor RMS current is derived from the switching states of space vector pulse width modulation (SVPWM). The expression is a function of the modulation index and power factor, and can be used to estimate the maximum dc-link capacitor RMS current. Both simulation and experimental results are presented to validate the accuracy of the proposed model and the derived expression of the dc-link capacitor RMS current.**

Keywords—Multilevel converter, Dc-link capacitor, Modulation.

I. INTRODUCTION

Three-phase voltage source inverters (VSIs) play an important role in various applications [1]-[3]. The VSIs can be generally classified into two major categories based on the number of output voltage levels, i.e., two-level and multilevel VSIs. Compared to two-level (2-L) inverters, multilevel inverters can generate output voltage with lower total harmonic distortion (THD) which may lead to a significant reduction on the volume and cost of active filters as well as the voltage stress on the switches [4], [5].

Three-level (3-L) inverters are the most widely used multilevel inverters due to their simple topology and control strategy [6], [7]. Several studies on 3-L inverters have been done in neutral-point voltage balancing and modulation strategy design [8]. Similar with 2-L VSIs, the space-vector pulse width modulation (SVPWM) has been proved to be an effective modulation strategy for 3-L inverters [9], and various new SVPWM algorithms have been proposed to improve the properties of the inverters [10], [11].

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When designing a 3-L VSI, in addition to selecting the proper circuit topology and modulation scheme, the dc link capacitors should also be sized and selected properly. On one hand, an oversized dc link capacitor can withstand higher root-mean-squire (RMS) current than the required value, which however will increase the volume of the VSI system and lower the power density. On the other hand, if dc link capacitor bank is tightly designed, due to the equivalent series resistances (ESR), the dc link current can overheat the capacitors and reduce the system reliability.

A detailed discussion on RMS value calculation of the dc-link capacitor current calculation for 2-L inverters has been presented in [12] and the influence of ac current ripple on the dc-link current has been studied in [13] based on the current ripple prediction method. Similar work for 3-L inverters has been done in [14]. The method presented in [14] was based on the assumption that ac ripple components in the dc-link current only flows into the dc-link capacitor, thus dc-link capacitor current can be estimated based on dc-link currents. However, this assumption may not be always valid since part of the ac ripple may flow back to the voltage source and thus introduces estimation errors. In addition, the expressions presented in [14] are too complicated for practical applications to be adopted. Therefore, it is critical to develop an accurate model for dc-link capacitor current as well as its RMS value calculation, which however cannot be found in the existing literature.

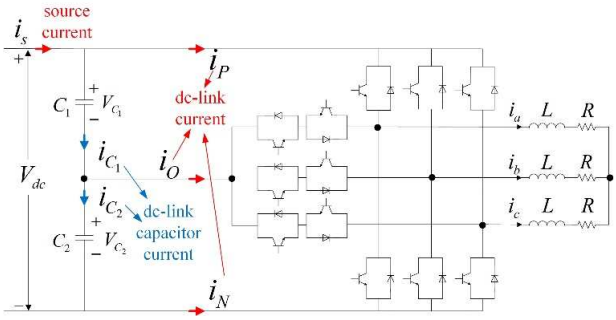


Fig. 1. The topology of a typical T-type 3-L VSI.

In this paper, a generic approach for the dc-link capacitor current modeling and its RMS value calculation for 3-L inverters are proposed. In this work, all the modeling and analysis are presented based on a T-type inverter using the four-region three-level SVPWM [15]. However, the proposed method can be applied to another 3-L inverter topology with different SVPWM pattern. The modeling and analysis of dc-link current and dc-link capacitor current are presented in Section II. The RMS value calculation for dc-link capacitor current is given in Section III. The validation using Matlab/Simulink and experimental studies are provided in Sections IV, and the final conclusions are illustrated in Section V.

II. DC-LINK CAPACITOR CURRENT MODELING

The topology of a typical 3-L T-type inverter with resistive-inductive (*RL*) load is shown in Fig. 1. DC-link capacitors C_1 and C_2 are usually selected to be the same, i.e., $C_1 = C_2 = C$, such that they can equally share the voltage across the dc-link V_{dc}. The currents flow through the top and bottom capacitors can be determined as

$$i_{C_1} = C\frac{\mathrm{d}V_{C_1}}{\mathrm{d}t} \tag{1}$$

$$i_{C_2} = C\frac{\mathrm{d}V_{C_2}}{\mathrm{d}t} \tag{2}$$

respectively. Assuming V_{dc} is approximately constant, the summation of these two capacitor currents is

$$i_{C_1} + i_{C_2} = C\frac{\mathrm{d}\left(V_{C_1} + V_{C_2}\right)}{\mathrm{d}t} = C\frac{\mathrm{d}\left(V_{dc}\right)}{\mathrm{d}t} \approx 0 \tag{3}$$

The other relationship between these two capacitor currents can be obtained using Kirchhoff's current law (*KCL*) at the mid-point of the dc-link

$$i_{C_1} - i_{C_2} = i_O \tag{4}$$

where i_O is the current through the middle dc-link wire. Based on to (3) and (4), it can be found that

$$i_{C_1} = -i_{C_2} = \frac{i_O}{2} \tag{5}$$

There are three switching states for a phase-leg in a 3-L inverter, i.e., P-, O-, and N-state, corresponding to the phase voltage at inverter output terminal with respect to the negative rail of the dc bus as V_{dc}, V_{dc} /2 and 0, respectively. Defining the middle wire switching state s_k for phase k (k = a, b, or c) as s_k = 1 when phase k is operated in O-state, otherwise as s_k = 0. Then based on *KCL*, i_O can be expressed as

$$i_O = s_a i_a + s_b i_b + s_c i_c \tag{6}$$

where i_a, i_b and i_c are the 3-phase load currents. Further considering the *KCL* at the neutral point in the load side

TABLE I. SWITCHING STATES VS. DC-LINK CAPACITOR CURRENT

$[s_a\ s_b\ s_c]$	$i_{c1}(=-i_{c2})$	$[s_a\ s_b\ s_c]$	$i_{c1}(=-i_{c2})$
[0 0 0]	0	[1 0 0]	$i_a/2$
[0 0 1]	$i_c/2$	[1 0 1]	$-i_b/2$
[0 1 0]	$i_b/2$	[1 1 0]	$-i_c/2$
[0 1 1]	$-i_a/2$	[1 1 1]	0

$$i_a + i_b + i_c = 0 \tag{7}$$

the instantaneous dc-link capacitor currents under different switching combinations can be obtained and are summarized in Table I.

III. DC-LINK CAPACITOR RMS CURRENT CALCULATION

With the above dc-link capacitor current model, the common RMS current $I_{C,rms}$ can be obtained as

$$I_{C,rms} = I_{C_1,rms} = I_{C_2,rms} = \frac{I_{O,rms}}{2} \tag{8}$$

where $I_{O,\mathrm{rms}}$ is the RMS current in the middle wire of the dc-link. To determine the $I_{O,\mathrm{rms}}$ over a switching period or a fundamental period, the load currents with balanced 3-L *RL* load and high frequency harmonics neglected can be expressed as

$$\begin{cases} i_a = I_N\cos\left(\theta+\varphi\right) \\ i_b = I_N\cos\left(\theta-2\pi/3+\varphi\right) \\ i_c = I_N\cos\left(\theta+2\pi/3+\varphi\right) \end{cases} \tag{9}$$

where I_N is the peak value of average current, φ is the load phase angle, and θ is the time-variable angle with the fundamental frequency f_N as

$$\theta = 2\pi f_N t \tag{10}$$

Then the rms current can be derived based on the 3-L SVPWM pattern.

A. 3-L SVPWM

A typical 4-region space vector diagram for 3-L SVPWM is given in Fig. 2. The vector space is divided into six triangular sectors and each sector is further divided into 4 regions. The reference voltage vector can be expressed as

$$\vec{V}_{ref} = V_N e^{j\theta} \tag{11}$$

where V_N is the magnitude of the reference voltage. When the reference vector sweeps across each region, at any specific time instant, the operating periods of the three nearest vectors can be calculated by using volt-sec balancing. The modulation index m_a is defined as

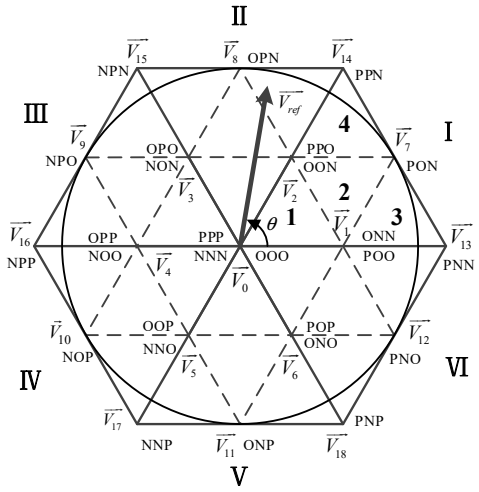


Fig. 2. Four-region 3-level SVPWM diagram

$$m_a = \frac{\sqrt{3}V_N}{V_{dc}} \tag{12}$$

Within linear modulation region, the maximum value for V_N is $V_{N,\max} = \sqrt{3}V_{dc}/3$, which equals to the radius of inscribed circle of the hexagon shown in Fig. 2 and thus the range of m_a is limited to $0 \le m_a \le 1$.

B. RMS Calculation for Dc-link Capacitor Current

Considering the symmetry of the pattern, Sector I is selected as an example, when m_a increases, V_N also increases and reference voltage may sweep across different regions in Sector I, which is illustrated in Fig. 3. In this work, the RMS current calculation are discussed in three cases depending on the value of m_a, i.e., $0 \le m_a \le \frac{1}{2}$, $\frac{1}{2} < m_a \le \frac{\sqrt{3}}{3}$ and $\frac{\sqrt{3}}{3} < m_a \le 1$, and the detailed calculation procedure for the 2nd case, as shown in Fig. 3(b), is presented. The calculations for other cases care similar.

In Fig. 3(b), the value marked in the bracket after each vector describes the contribution of this vector to the RMS current in the middle wire of the dc-link, i.e., $I^2_{O,rms}$. Since the reference vector sweeps cross both Regions 1 and 2, the calculations should be divided into two parts: the operating range Γ_1 in Region 1, which consists of both $[0, \beta_1]$ and $[\pi/3 - \beta_1, \pi/3]$, and the operating range Γ_2 in Region 2, which consists of $[\beta_1, \pi/3 - \beta_1]$, where β_1 can be obtained as

$$\beta_1 = \arcsin\left(\frac{1}{2m_a}\right) - \frac{\pi}{3} \tag{13}$$

Over Γ_1, the middle dc link RMS current over one switching cycle is

$$i_{O,rms,1} = \sqrt{\frac{1}{T_s}\left(\lambda_{\vec{V}_1} i_a^2 + \lambda_{\vec{V}_2} i_c^2\right)} = \sqrt{\frac{T_a}{T_s} i_a^2 + \frac{T_c}{T_s} i_c^2} \tag{14}$$

where $\lambda_{\vec{V}_i}$ $(i = 0, 1, 2, ..., 27)$ is the operating time of vector $\vec{V}_i$ in one switching cycle. Then over Γ_1,

$$\int_{\Gamma_1} i^2_{O,rms} d\theta = \int_0^{\beta_1} i^2_{O,rms,1} d\theta + \int_{\pi/3-\beta_1}^{\pi/3} i^2_{O,rms,1} d\theta \tag{15}$$

Substituting (9) and (14) into (15) yields (16). Similar to the calculation over Γ_1, (17) can be obtained over Γ_2. Since the RMS current over one fundamental period can be expressed as

$$I^2_{O,rms} = \frac{6}{2\pi}\int_0^{\pi/3} i^2_{O,rms} d\theta = \frac{3}{\pi}\left(\int_{\Gamma_1} i^2_{O,rms} d\theta + \int_{\Gamma_2} i^2_{O,rms} d\theta\right) \tag{18}$$

Substituting (16) - (18) into (8) yields (19). (16), (17) and (19) are all located at the bottom of this page.

Equation (19) is only valid for the 2nd case. Following the same procedure, $I_{C,rms}$ can be determined for other two cases shown in Fig. 3. After the calculations for all three cases, can be described using a general expression as

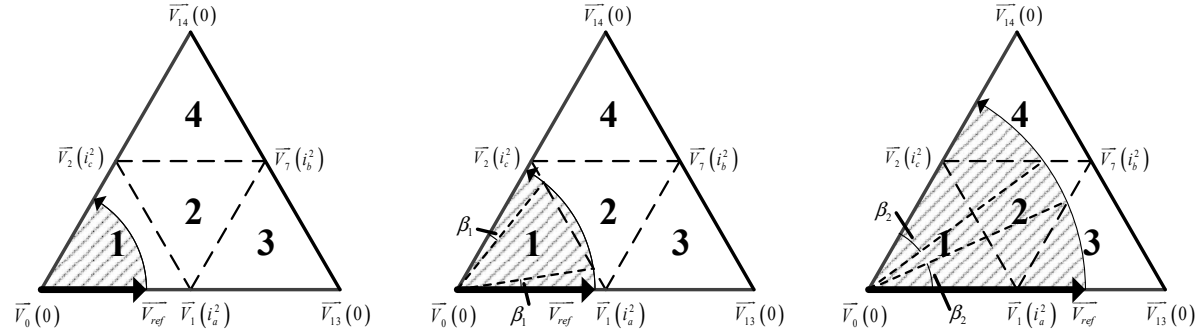


Fig. 3. Regions swept by reference voltage for (a) $0 \le m_a \le \frac{1}{2}$, (b) $\frac{1}{2} < m_a \le \frac{\sqrt{3}}{3}$, and (c) $\frac{\sqrt{3}}{3} < m_a \le 1$.

$$\int_{\Gamma_1} i^2_{O,rms} d\theta = I_N^2 m_a \left\{1 - 2\cos\left(\beta + \frac{\pi}{3}\right) + \left[\frac{2}{3} - 2\sin\left(\frac{\pi}{6} - \beta\right) + \frac{1}{3}\cos 3\beta\right]\cos 2\varphi\right\} \tag{16}$$

$$\int_{\Gamma_2} i^2_{O,rms} d\theta = I_N^2 \left\{\frac{\pi}{6} - \beta + \left[\sin\left(\frac{\pi}{3} - 2\beta\right) - m_a \cos 3\beta\right]\cos 2\varphi\right\} \tag{17}$$

$$I_{C,rms} = I_N \sqrt{\frac{3}{4\pi}\left\{\frac{\pi}{6} - \beta + \sin\left(\frac{\pi}{3} - 2\beta\right)\cos 2\varphi + m_a\left[1 - 2\sin\left(\frac{\pi}{6} - \beta\right) + \left[\frac{2}{3} - 2\sin\left(\frac{\pi}{6} - \beta\right) - \frac{2}{3}\cos 3\beta\right]\cos 2\varphi\right]\right\}} \tag{19}$$

TABLE II. EXPRESSIONS OF A, B, C AND D IN (20)

m_a	β	A	B	C	D
$0 \le m_a \le \frac{1}{2}$		2/3	1	0	0
$\frac{1}{2} < m_a \le \frac{\sqrt{3}}{3}$	$\arcsin\left(\frac{1}{2m_a}\right)-\frac{\pi}{3}$	$\frac{\pi}{3}-2\sin\left(\frac{\pi}{6}-\beta\right)-\frac{2}{3}\cos 3\beta$	$1-2\sin\left(\frac{\pi}{6}-\beta\right)$	$\sin\left(\frac{\pi}{3}-2\beta\right)$	$\frac{\pi}{6}-\beta$
$\frac{\sqrt{3}}{3} < m_a \le 1$	$\frac{\pi}{3}-\arcsin\left(\frac{1}{2m_a}\right)$	$\frac{\pi}{3}-2\sin\left(\frac{\pi}{6}+\beta\right)-\frac{2}{3}\cos 3\beta$	$1-2\sin\left(\frac{\pi}{6}+\beta\right)$	$\sin\left(\frac{\pi}{3}-2\beta\right)$	$\frac{\pi}{6}-\beta$

$$I_{C,rms} = I_N \sqrt{\frac{3}{4\pi}\left[\left(Am_a + B\right)\cos 2\varphi + \left(Cm_a + D\right)\right]} \quad (20)$$

where the values of parameters A, B, C and D are listed in Table II.

C. Peak Value of Dc-link Capacitor RMS Current

With the impedance of the load marked as Z, the unit current value is defined as

$$I_{base} = \frac{V_{dc}}{Z} \quad (21)$$

and the 3D curve of $I^*_{C,rms} = I_{C,rms} / I_{base}$ verses cosφ and m_a is given in Fig. 4. For each power factor, the peak RMS current occurs when

$$\frac{\mathrm{d}I_{C,rms}}{\mathrm{d}m_a} = 0 \quad (22)$$

is satisfied and the maximum dc-link capacitor RMS current track can be marked as shown in Fig. 4. From the track it can be seen that when cosφ < 0.68, the maximum RMS dc-link capacitor current points locate at m_a = 1, or the output RMS voltage reaches maximum value, however, when cosφ > 0.68, as cosφ increases, the maximum RMS current dc-link capacitor current points locate at a smaller m_a than unity and thus the DC-link capacitors should be selected with care based on the track to avoid overheat situations. Also, the dc-link capacitors should operate with lower RMS current to increase the reliability.

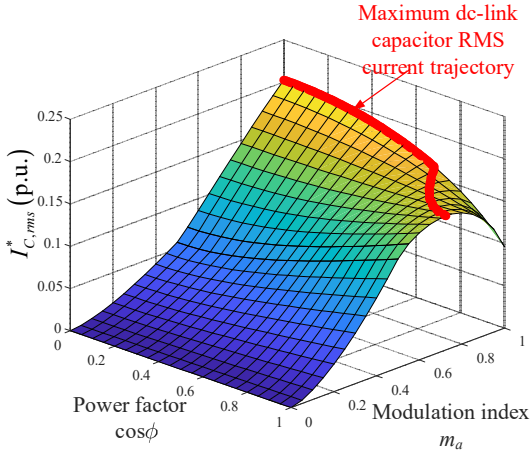
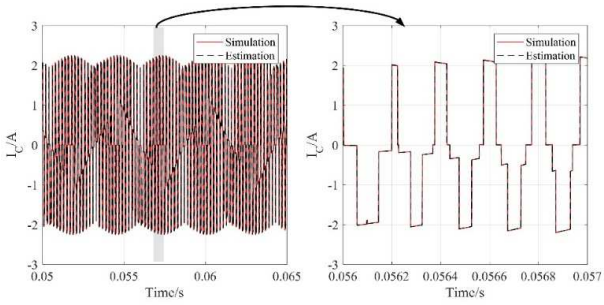


Fig. 4. Normalized dc-link capacitor RMS current vs. power factor and modulation index.

IV. SIMULATION AND EXPERIMENTAL STUDIES

A. Simulation Results

To validate the correctness and effectiveness of the proposed dc-link capacitor current model as well as its RMS calculation approach, both simulation and experimental studies are performed. A T-type 3-L inverter with RL load using SVPWM is simulated in Matlab/Simulink with V_{dc} = 100 V, R = 10 Ω and L = 4 mH. With m_a = 0.8 and switching frequency f_{sw} = 5 kHz, both simulated and estimated dc-link capacitor current waveforms are shown in Fig. 5. These two waveforms match with each other well. Using the same load and varying m_a from 0.01 to 1, simulated and estimated RMS current using both proposed method and method presented in [14] are compared in Fig. 6. It can be seen that the accuracy of the proposed approach is high, and the error between the proposed approach and simulation result is less than 3%.



(a) (b)

Fig. 5. Simulated and estimated waveforms for dc-link capacitor current (a) over a fundamental cycle and (b) zoomed in results.

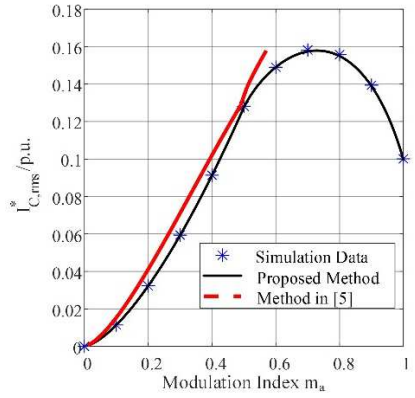


Fig. 6. A comparison between the estimated and simulated dc-link capacitor RMS current vs. m_a.

B. Experimental Validation

A 3-L T-type inverter prototype using Cree silicon carbide (SiC) Power MOSFETs C2M0160120D as shown in Fig. 7 was utilized to perform the experimental study. The circuit parameters are the same as those used in the simulation study. The SVPWM gate signals were generated by a dSPACE MicroLabBox RTI1202. A Pearson™ 20 MHz bandwidth current monitor (Model 411) is used to measure the dc link capacitor current.

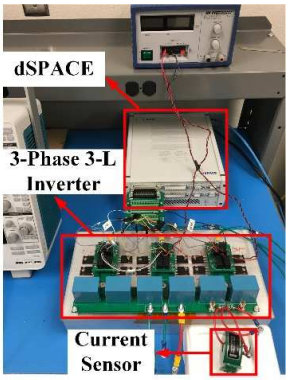
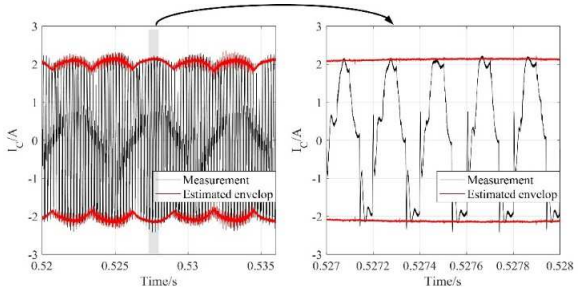


Fig. 7. Experimental test setup.



(a) (b)

Fig. 8. The measured and estimated waveforms for dc-link capacitor current (a) over a fundamental cycle and (b) zoomed in results.

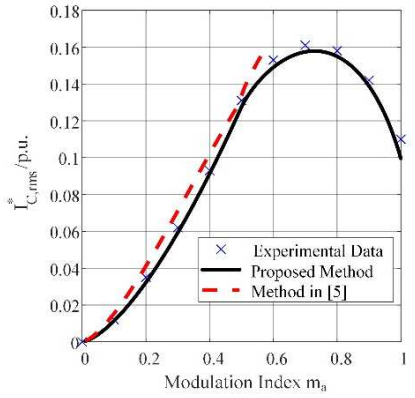


Fig. 9. Comparison between the estimated and simulated dc-link capacitor RMS current vs. m_a.

In the experimental study, the proposed dc-link capacitor current model and sense load currents were used to determine maximum and minimum of the dc link capacitor current in each switching cycle, which led to the estimated envelop of dc-link capacitor current. The measured dc-link capacitor current and the estimated envelope of the dc-link capacitor current are shown in Fig. 8. The estimated envelop matches the measured waveform with a small error due to the ripple caused by the parasitic of the inverter circuit, especially the dc-link capacitor. The measured RMS current, estimated RMS current based on (20) as well as the method presented in [14] are shown in Fig. 9. The proposed approach shows improved accuracy and at the same time in a significantly simplified form, which is more convenient to use in practical application.

V. Conclusions

In this work, an accurate dc-link capacitor current model and its RMS value calculation approach are proposed for 3-L VSIs. The dc-link capacitor currents are determined using the current in the middle wire of the dc-link, which further lead to an expression for the dc-link capacitor current rms value. Based on this expression, the maximum dc-link capacitor RMS current trajectory is given, which is critical to properly size the dc-link capacitors to increase life span and power density. The proposed method can be generalized to other multilevel inverters. With the verification of both simulation and experimental studies, this expression has not only simplified expression, but also improved accuracy compared to the existing approach.

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