Lutz v. Wangenheim
June 2020

Double Integrator Oscillator (DIO) - why does it oscillate?

„Curiously, this is an exceptional oscillator which does not appear to fail to start in spite of this apparent difficulty“ (R. Senani et al: „Sinusoidal Oscillators and Waveform Generators using Modern Electronic Circuit Building Blocks“, Springer Int. Publishing, 2016)

***

Introduction

If the classic inverting integrator stage (*MILLER* integrator, phase shift +90 deg) is connected in a closed loop with a non-inverting integrator circuit (phase shift -90 deg), see Fig.1, the phase shifts of both stages compensate each other - and this combination of two integrators is able to oscillate continuously. For realizing the non-inverting integrator a *MILLER* integrator with an additional inverter can be used.

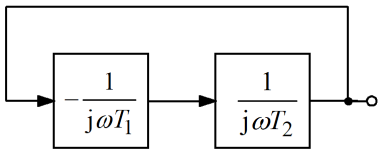

Fig.1 Double-Integrator loop, Block Diagram

Thus, the oscillation condition (*BARKHAUSEN*) seems to be fulfilled - and the oscillation frequency *f*o follows from the loop gain condition:

$$\underline{L}_0(j\omega_0) = -\frac{1}{j\omega_0 T_1}\cdot\frac{1}{j\omega_0 T_2} = \frac{1}{\omega_0^2 T_1 T_2} = 1,$$

$$\Rightarrow \quad f_0 = \frac{1}{2\pi\sqrt{T_1 T_2}} \xrightarrow{T_1=T_2=T} \frac{1}{2\pi T}.$$

So - what's the problem with this "Double Integrator Oscillator (DIO)"? What is the background for the question in the title?

As can be seen, the loop gain is always real (zero phase). This means that the phase condition for oscillation is fulfilled for all frequencies. And that is the problem because we require that the oscillation condition (magnitude and phase) must be fulfilled at one single frequency only!

Fortunately, the world of electronics is a real world and the equations as given above assume ideal integrating functions and, in particular, **ideal** opamps.

However, for integrating stages with **real** amplifiers, a phase shift of exactly 90 deg does exist at one single frequency only. So - is that the frequency at which the circuit can oscillate? The discussion of this problem is continued in form of a realistic example.

Example

Simulation results of a *MILLER* integrator for a realistic opamp macro model (LM741) with the time constant $T=RC=159.15\mu s$ is shown in Fig.2 (*BODE* diagram).

The cross-over frequency f_{co} (0 dB gain) is identical with the desired oscillation frequency $f_o=1/2\pi T=1$ kHz. At this frequency, the corresponding phase angle of +89.9 deg is taken from the magnified phase response (upper part of Fig. 2). Hence, we have a phase error of -0.1 deg and the ideal value of 90 deg is achieved at a frequency as low as $f_{90}\approx 70$ Hz only.

This raises the question of whether two non-ideal *MILLER* integrators (together with a unity-gain inverter) in a closed loop could generate a continuous oscillation at f_o=1 kHz, although a phase error about twice as large can be expected for the two stages (app. -0.2 deg).

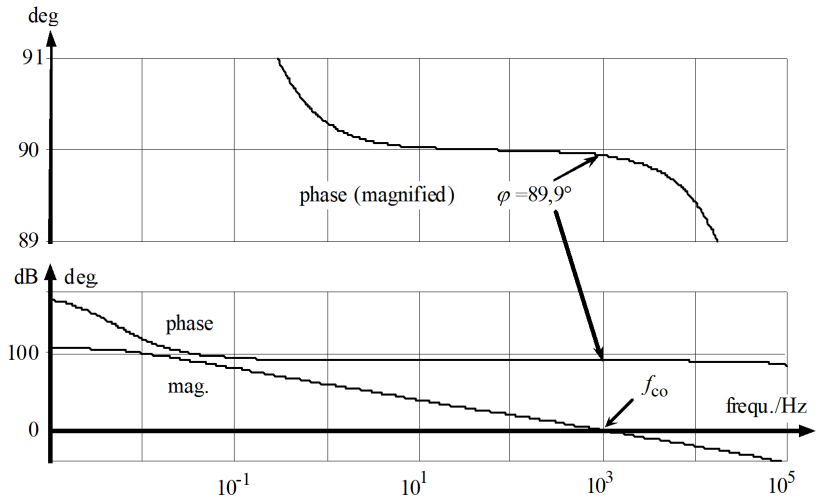

Fig.2 Integrator (inverting), real opamp model, magnitude and phase response

First of all, it should be noted that at f_{90}≈70 Hz the gain of each integrator is far above 0 dB. Therefore, the loop consisting of two integrators (plus inverter) will have a gain larger than unity with zero phase at this frequency. This condition initially ensures a safe start of oscillations (self-excitation) until the rising signal amplitudes reach the dynamic range limits of the opamps.

More than that, it can be demonstrated both experimentally and by simulation that a stationary oscillation state is established at the design frequency of f_o=1kHz - with a surprising good signal quality (low THD).

Simulation results (3 opamps LM741, supply: +-9V, T_1=T_2=10k*15.9nF=159.15µs):

Loop phase error (at f_{co} =0.998kHz): -0.23 deg; THD≈0.35%.

Explanation

This observation deserves some explanations.

It can be shown that the negative phase error of -0.23 deg will be compensated by a positive phase shift, which is caused by non-linear overdrive effects of both integrating blocks as soon as the amplitudes reach the limits of the opamps dynamic range.

Thus, at a certain level of amplifier overdrive (with limitation of signal amplitudes), a state of equilibrium is established automatically between the system-induced negative phase error and the positive phase shift which depends on the degree of overdrive.

This effect can be made visible by circuit simulation (Fig. 3). For this purpose, two otherwise identical *MILLER* integrators are operated with different supply voltages (12 V or 6 V). Both units have a time constant T=159.15 µs and receive the same input signal with a frequency f=1 kHz. The selected signal input amplitude (10 V) will only overdrive amplifier No. 2 (6 V supply voltages).

A comparison of the two output signals reveals that the signal at output 2 is 50 µs ahead of output 1 (corresponding to app. +18 deg) which is caused by severe signal clipping.

In practice, however, the overdrive effects are much smaller, since the phase deviations to be compensated rarely exceed a limit of some degrees. In our simulation example, the negative phase error for the DIO of only -0.23 deg results in a rather small signal limitation at the output.

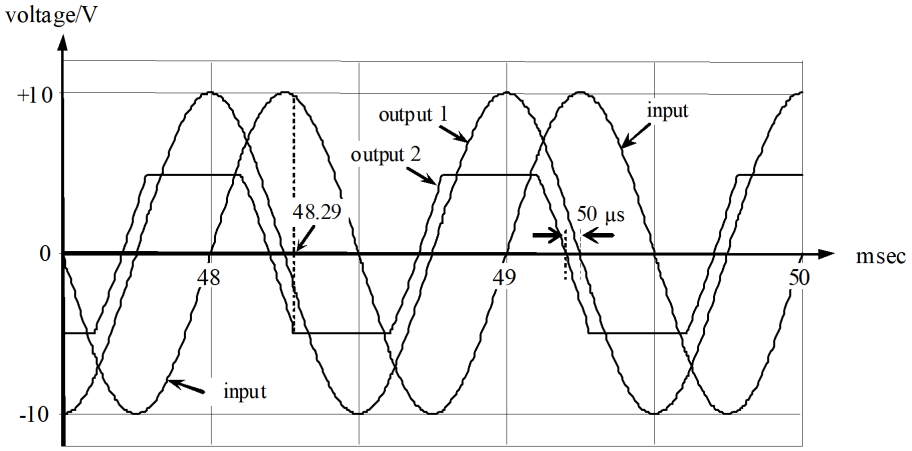

Fig.3 Integrator (inverting): output 1 without overdrive, ouput 2 with overdrive (clipping)

Detailed explanation

As a result of negative feedback, the "virtual ground" principle is effective for the inverting opamp input as long as the amplifier can operate in the linear operating range. However, as soon as the maximum signal output (limited by the supply voltages) is reached, the negative feedback becomes ineffective.

As a result, the capacitor charge is altered further (increased/decreased, depending on the input phase) directly by the input voltage via the integration resistor ("from the other side") - and no longer by the output voltage of the amplifier. In this time interval the voltage at the inverting input consists of small positive or negative "half waves".

If, for example, the amplifier output is on the negative limit, the capacitor is further charged by the positive half-wave. When the opamp then returns to the linear range in the following half-wave, this additional charge leads to a shift of the half-wave output voltage "upwards", which means a shift to the left - equivalent to a positive phase shift.

Discussion and Outlook

With the exception of very large time constants ($T>1/\omega_p$) the phase shift of inverting integrator units realized with real amplifiers (DC gain app. 1E5; first pole at ω_p) will always cross the +90 deg line at a frequency f_{90} which is below the frequency of interest ($f=f_{co}$), where the gain of the integrator is 0 dB ($f_{90}<f_{co}$). Thus, the phase error at f_{co} has always a negative sign. A rough calculation for a first-order opamp model leads to the relation $\omega_{90}=\mathrm{sqrt}(\omega_p/T)$.

We can, therefore, expect that there is always a frequency below the expected oscillation frequency *fo* where the loop gain of the DIO has zero phase shift and a corresponding loop gain >0 dB. This ensures start of oscillations with rising amplitudes.

For increasing frequencies the phase error (in our example: -0.23 deg) can be much larger (up to several degrees!), but the circuit will, nevertheless, be capable to oscillate - with more clipping effects - at a frequency, where the loop gain criterion seems not to be fulfilled (small-signal loop gain magnitude zero with a negative phase error).

The phase difference between both oscillator signals is 90 deg, from which the commonly used term "quadrature oscillator" is derived. For equal time constants $T_1=T_2$ and equal supply voltages both opamps will reach the maximum possible amplitudes at the same time and, therefore, will exhibit equal limiting effects (which, however, are hardly visible in our example).

However, according to the equation for the oscillating frequency f_o both time constants can also be selected unequal. Then, the two stages no longer have the same amplification at f_o - with the consequence that only one stage (larger amplification, smaller time constant) will suffer from these limiting effects. The other stage delivers a smaller sinusoidal signal with an improved signal quality (filtering effect, damping of harmonics).

Simulation results (3 opamps LM741, supply: +-9V; T_1=1.25k*15.9nF; T_2=80k*15.9nF:
Loop phase error (at f_{co} =0.998kHz): -0.23 deg; THD (output 2)≈0.18%.

From this, we can conclude that it is always advisable to select unequal time constants for the integrator stages. The good quality of the smallest signal makes - in some cases - additional amplitude control unnecessary. It is another question, however, how such an automatic amplitude control mechanism could look like. In contrast to other oscillator topologies, it must be phase-sensitive and not gain-sensitive. One simple method could be to somewhat reduce the phase error value using a large resistor in parallel to the feedback capacitor of stage 1 (smaller time constant T_1, limited output). The value of this resistor must be carefully selected because the loop phase at f_{co} must remain slighly negative. (Analogy to the gain requirement for other oscillators: Loop gain must slightly be above unity).

In the example discussed above, a 500k resistor in parallel to the feedback capacitor results in a loop phase error of -0.068 deg only - with a consequence of a barely noticeable clipping effect. The harmonic distortion at output 2 is now reduced to THD≈0.07%.

***

Finally, it should be mentioned that - to the author's knowledge - the effect of phase shifting caused by integrator overdrive has not yet been mentioned in the technical literature. Many papers and articles have been published on integrator-based oscillators, but - unlike all other oscillator types - the keywords "amplitude" or "signal quality" have not been addressed. This also applies to technical books about filters and oscillators.

*