A High-Efficiency CMOS Rectifier for Low-Power RFID Tags

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***Abstract*—In this paper, a high-efficiency highly sensitive CMOS rectifier for radio-frequency identification (RFID) tags is presented. Although the minimum RF input signal amplitude for which the rectifier operates properly is lower than the standard threshold voltage of the MOS transistors, the design uses only standard-threshold-voltage (standard-V_{th}) devices. Furthermore, two rectifier biasing schemes are proposed. The first biasing scheme is intended for semi-passive RFID tags and allows the tag rectifier to adjust the input power level at which the rectifier's maximum power efficiency is achieved, i.e., the rectifier circuit can be tuned to achieve its maximum power efficiency at any given input power. The second biasing scheme is for self-sufficient rectifiers used in passive tags and does not require any auxiliary power source. The rectifier is designed and laid out in a standard 0.13-µm CMOS process and its performance is confirmed through post-layout simulations.**

I. INTRODUCTION

Radio-frequency identification (RFID) tags are typically classified into the following three general categories [1]: active, semi-passive, and passive tags. Active and semi-passive tags use an external battery as a sole or partial source of power for the tag circuitry. They support a high to moderate communication range to the base station (reader). The drawback of these tags is that the external battery adds to the weight and volume of the tag, makes it more expensive, limits the tag longevity, and reduces the reliability because of possible battery failures. On the other hand, passive tags operate without a battery. They use a rectifier block to extract their power from the transmitted RF signal (from the reader). Thus, passive tags are smaller, less costly, and usually more reliable than their active and semi-active counterpart. However, due to the limit on the maximum transmit power (e.g., 4W for electronic product code (EPC) protocol in North America [2]), passive tags suffer from a limited communication range. To increase this operating range the sensitivity and/or efficiency of the tag rectifier has to be improved so that the tag can efficiently extract power from a weak received RF signal.

Rectifier circuits for RFID tags are usually Dickson-based rectifiers [3] and designed either by Schottky diodes [4, 5] or CMOS transistors [1, 6-10] (since RFID applications are typically cost and area sensitive, often the tag circuitry is implemented in CMOS due to high level of integration and low cost of CMOS technology [6,7]). Schottky-diode rectifiers generally achieve a better performance due to the small turn-on voltage of the diodes. However, Schottky diodes are not readily supported in all CMOS technologies and therefore are not suited for CMOS implementations [6]. On the other hand, in CMOS technology the voltage drop of a diode-connected transistor is about the threshold voltage (V_{th}) of the MOS device. This voltage drop can be reduced either by including a fixed voltage source between the drain and gate of diode-connected transistors to reduce their turn-on voltage (static V_{th} cancelation) [1, 8, 9] or in more advanced technologies by using zero or low-V_{th} devices [10]. Both approaches increase the reverse leakage of transistors when the transistors must be turned off and thus reduce the efficiency of the rectifiers.

In [6, 7] a "four-transistor-cell" CMOS rectifier is proposed (Fig. 1(a)) which outperforms CMOS diode-based rectifiers, even when static V_{th}-cancelation technique is used to reduce the turn-on voltage of the diodes. In this circuit, the on-resistance of the transistors is decreased by increasing gate-source voltage ($|V_{GS}|$) of the transistors and the reverse leakage is reduced by reversing the polarity of the V_{GS} in the cross-coupled structures (Fig (a)). One drawback of the four-transistor-cell rectifier is that it does not perform well when the received RF power is weak (e.g, a few µW). This problem becomes more pronounce in lower-cost CMOS technologies where V_{th} of transistors is relatively high and the transistors do not turn on completely (the rectifier efficiency drops dramatically).

Fig. 1(b) shows the four-transistor-cell output voltage as a function of the effective V_{th} (threshold voltage of a transistor with a series voltage source in its gate (Fig. 1(c)) and of the transistors, for a given input power. As it can be seen from the figure, in the four-transistor- cell there is an optimum value for V_{th} (assuming $V_{th,n}$, $V_{th,p}$) that maximizes the output DC voltage for a given input power (this value is proportional to the input power). When the received RF power is low, the transistors with large V_{th} do not switch completely which results in higher output resistance and lower output voltage. If V_{th} is too small, then there is a large reverse leakage which also decreases the power conversion efficiency (PCE) of the rectifier. In [6], the use of floating gate transistors is suggested to adjust the threshold voltages of transistors at the cost of larger die area and larger input capacitance. As mentioned in [6], most currently available CMOS processes do not offer two poly layers, and therefore, implementation of the suggested floating gates is not practical.

In this paper, a simple auxiliary driver stage is proposed that drives the gates of the rectifier transistors with almost the

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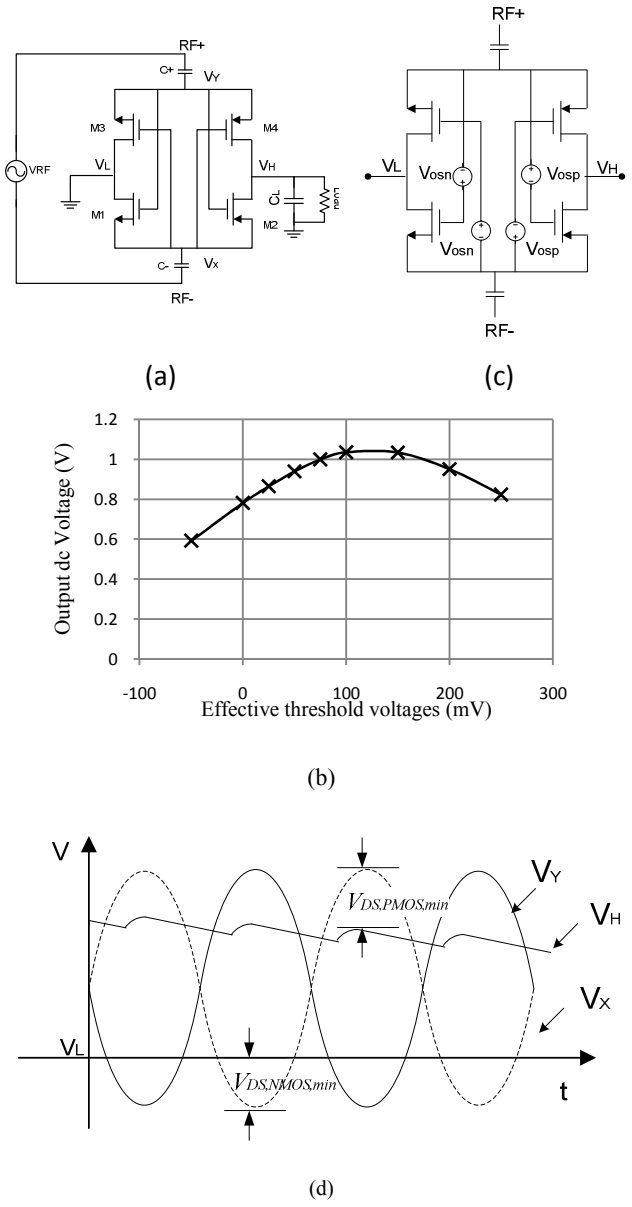


Fig 1. (a) Four-transistor cell (b) Output voltage of the rectifier for a given input power as a function of effective threshold voltage of transistors ($V_{th,n} = V_{th,p}$). (c) Changing the effective V_{th} of transistors in a four-transistor cell. (d) Node voltages in a four transistor cell

same amplitude as that of the input RF signal, however, with an adjustable DC level. The proposed circuit (shown in Fig. 2) is similar to the four-transistor-cell structure (Fig. 1(c)) in which to control the effective threshold voltage of each transistor a DC voltage source is connected in series with the gate of the transistor. Decreasing effective V_{th}, in turn, decreases the minimum amplitude of the input RF signal that is required for proper operation of the rectifier, and therefore, results in increased operation range of the RFID tag.

This paper is organized as follows. A high-efficiency highly sensitive rectifier circuit is presented in Section II. Two different rectifier biasing schemes are presented in Section III. The first scheme is intended for semi-passive RFID tags and allows the tag rectifier to adjust the input power level at which the rectifier's maximum power efficiency is achieved, i.e., the rectifier circuit can be tuned to achieve its maximum power efficiency at any given input power. The second biasing scheme is for self-sufficient rectifiers used in passive tags and does not require any auxiliary power source. The proposed highly sensitive and efficient rectifier along with the second biasing scheme for passive RFID tags are designed and implemented in a 0.13-µss CMOS technology. Post-layout and schematic level simulations of these circuit blocks are presented in Section IV. Finally, Section V concludes the paper.

II. PROPOSED CMOS RECTIFIER

As discussed earlier, Fig. 1(a) shows a conventional four-transistor-cell connected to a sinusoidal RF voltage source with amplitude equal to V_{RF}. C_L is the decoupling capacitor that is typically used to reduce the ripple on the output voltage (V_H) and is continuously discharges by the load. V_L terminal (which is connected to ground in Fig. 1(a)) is either connected to ground (in the first stage) or is a dc voltage generated by preceding rectifier stage (when this structure is used in a multi-stage rectifier).

In this stage, when RF+ becomes greater than RF-, transistors M_1 and M_4 turn on and M_2 and M_3 turn off. In this half cycle (refer to Fig. 1(d)), V_X is equal to $V_L - V_{DS1}$ where V_{DSi} denotes the drain-source voltage of transistor Mi. Meanwhile, some portion of the charge on the capacitor C+ charges C_L to $V_Y - |V_{DS4}|$. In the next half cycle, M_2 and M_3 turn on and M_1 and M_4 turn off. In this time interval, M_3 passes charge from ground to the capacitor C+ thus recharging C+, and some of the charge on capacitor C- moves to C_L. Note that $V_H = V_X - |V_{DS2}|$.

Let $V_{DS,min}$ denote the minimum $|V_{DS}|$ which occurs when the maximum gate-source voltage (~V_{RF}). In the steady-state, V_X and V_Y change from $V_L - V_{DS,NMOS,min}$ to approximately $V_L - V_{DS,NMOS,min} + V_{RF}$ with 180° phase difference. Thus, $V_{H,max} = V_L - V_{DS,NMOS,min} + V_{RF} - V_{DS,PMOS,min}$ (Fig. 1(d)). As long as V_{RF} is sufficiently larger than $|V_{th}|$, $V_{DS,min}$ remains small and the output voltage becomes approximately $V_L + V_{RF}$. However, for a given V_{RF}, if $|V_{th}|$ is too large, V_H becomes small, because of large $V_{DS,min}$ of transistors. On the other hand, when $|V_{th}|$ is too small, transistors conduct some current from C_L to C+ or C- before they completely turn off.

This undesired current drops the overall efficiency. Fig. 1(c) shows a four-transistor-cell with DC voltage sources connected in series with gate of the transistors (V_{osn} for NMOS and V_{osp} for PMOS). In this arrangement, the effective threshold voltage of the NMOS and PMOS transistors are $V_{th,n} - V_{osn}$ and $V_{th,p} + V_{osp}$, respectively. By proper selection of the offset voltages (V_{osn} and V_{osp}) the optimum value of $|V_{th}|$ at any given power can be achieved. In the circuit of Fig. 1(c), the gate voltage of the transistors changes from about $V_L + V_{osn}$ to $V_L + V_{osn} + V_{RF} \approx V_H + V_{osn}$ (assuming small voltage drops on the transistors).and from $V_L - V_{osp}$ to $V_L - V_{osp} + V_{RF} \approx V_H - V_{osp}$ for PMOS transistors.

In the proposed circuit (shown in Fig. 2) two drivers are utilized to drive the gates of the rectifier transistors (M_1-M_4) in a configuration similar to that of Fig. 1(c). Consequently, the proposed circuit and the circuit in Fig. 1(c) show almost

the same performance.

In Fig. 2 V_{BN} and V_{BP} are two bias voltages that mimic the function of V_{osn} and V_{osp}. Fig. 3 shows the drivers, connected to C_{load} that models the parasitic capacitances of the transistors in the driver and the transistors driven by the driver in the rectifier. At start up, and in the NMOS driver circuit when RF- becomes greater than RF+, M_1 turns on and M_2 turns off. At this time, M_1 conducts some charge from V_{B1} to the capacitor C_1 which is connected to its source. In the next half cycle, when M_1 is off and M_2 turns on, capacitor C_2 is charged through M_2. This process continues until the voltage on the capacitor becomes almost equal to V_{B1}. After that, M_1 and M_2 do not conduct any DC current, except for a small amount of leakage current. In the steady state, the minimum driver output voltage is,

$$V_{0,min} = V_{B1} - V_{D,M1,2} \quad (1)$$

where $V_{D,M1,2}$ is the voltage drop (drain-source voltage) of M_1 and M_2. The maximum output voltage of the drivers is therefore

$$V_{0,max} = V_{o,min} + V_{RF}.C_{1,2}/(C_{1,2} + C_{load}) \quad (2)$$

$C_{1,2}$ can be chosen big enough such that $C_{1,2}/(C_{1,2} + C_{load}) \approx 1$. This does not require a very large $C_{1,2}$ since C_{load} is the sum of the parasitic capacitances of the rectifier and driver transistors and therefore is rather small. In the PMOS driver when RF+ becomes larger than RF–, M_1 turns on and conducts charge to C_1 and in the next half cycle M_2 charges C_2. The output voltages (V_{o+} and V_{o-}) changes between

$$V_{o,max} = V_{B2} - V_{D,M1,2} \quad (3)$$

and

$$V_{0,min} = V_{o,max} - V_{RF}.C_{1,2}/(C_{1,2} + C_{load}) \quad (4)$$

Unlike the NMOS driver, the DC level of the PMOS driver outputs (i.e., PMOS driver output common-mode level) becomes less than V_{B2}. In Fig. 3, by setting the voltage sources V_{B1} and V_{B2} to

$$V_{B1} = V_L + V_{osn} \quad (5)$$

and

$$V_{B2} = V_H - V_{osp} \quad (6)$$

the values of the voltages applied to the gates of the rectifier transistors will be (approximately) the same as those in Fig. 1(c), and thus the two circuits will show (almost) the same performance.

Note that since drain currents of M_1 and M_2 can be very small, even RF voltage swings smaller than transistor V_{th} can properly charge the capacitors. This can be seen in Fig. 6 in Section IV, where the rectifier operates with RF voltage amplitudes smaller than threshold voltages (nominal threshold values of $V_{th,n}$ = 0.355 V and $V_{th,p}$ = −0.325V). The output

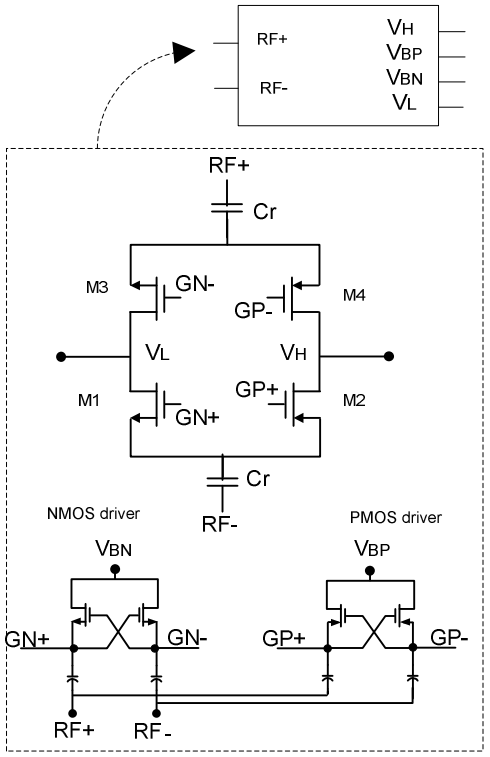


Fig 2. One "driven-gate" rectifier stage with NMOS and PMOS drivers. (The first stage does not have capacitors C_r).

voltage of the driver reaches the desired value even for V_{RF} amplitude as small as 280 mV which is smaller than the nominal V_{th} of the transistors.

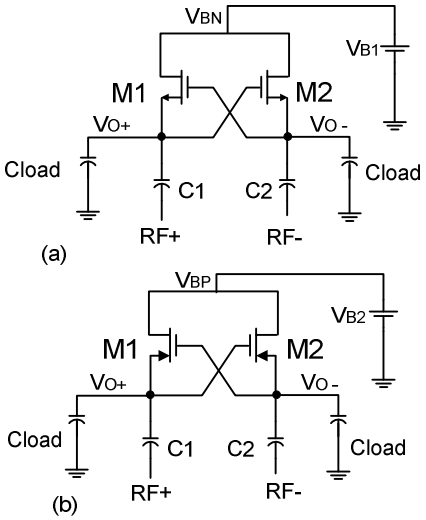


Fig.3 (a) NMOS driver (b) PMOS driver

To bias the rectifier transistors, NMOS drivers can be used for NMOS transistors of the rectifier and PMOS transistors can be used for PMOS transistors of the rectifier. However, in some technologies $V_{th,p}$ is considerably larger than $V_{th,n}$. Therefore, the transistors in PMOS drivers may not switch properly, which results in undesirable driver voltage levels. In this context, NMOS drivers are preferred over

PMOS drivers. To drive PMOS transistors with an NMOS driver, V_B of the i[th]-stage driver must be set to $V_{L,\,i} - V_{osp}$. The problem with using NMOS-only drivers is that for driving the PMOS transistors in the first rectifier stage, V_B of the driver must be $-V_{osp}$ which is negative and is lower than the ground voltage and its generation requires a complex circuitry. Connection of NMOS-PMOS drivers are shown in Fig. 2. We shall call the proposed rectifier with either NMOS or PMOS drivers, "driven-gate" rectifier.

III. BIASING CIRCUIT

In this section, two biasing schemes for generating V_{BN} and V_{BP} are presented. The first scheme is a switched-capacitor-based circuit and is intended for semi-passive tags, while the second scheme is a continuous-time technique and is intended for passive tags.

A. Switched-Capacitor Circuit

One way to create the bias voltages V_{B1} and V_{B2} in Fig. 3 is to connect a charged capacitor with initial voltage equal to the offset voltages V_{osn} and V_{osp} between V_L and V_H of each rectifier stage, respectively (Fig. 4). As mentioned earlier in Section II, the DC current through the biasing voltage sources is almost zero. In the beginning of the operation the driver capacitors (C_1 and C_2 in Fig. 3) draw some current from the bias voltage source (V_B). After that the current through those voltage sources drop to almost zero. Therefore, placing a large enough charged capacitor (C_{bias}) instead of V_{osn} and V_{osp} gives the desirable bias voltages (Fig. 4). C_{bias} must be recharged every once in a while since it is continuously discharged by a (small) leakage current, however, the recharging frequency can be as low as a few kHz.

Note that the leakage of the capacitors are negligible when metal-insulator-metal (MIM) capacitors are used, in which case, the only leakage is through transistors. The low recharging frequency is desirable since it reduces the overhead power of the biasing circuit and increases the overall efficiency of the rectifier. The biasing circuit is shown in Fig. 4. This technique enables the rectifier to change the value of V_{osn} and V_{osp} dynamically, and thus, allows for changing the input power that the maximum PCE occurs. However, it requires an initial voltage source at the power up to start operation and therefore is suitable for semi-passive tags. A small low-capacity battery should be included to supply the bias voltages when the biasing circuits are to startup for charging C_{bias} of different stages and switch the transistors in the recharging circuit.

B. Transistor Chain

In this biasing technique, a number of transistors are connected in series, (Fig. 5). The dimensions of the transistors in the chain determine the value of the bias voltages that are generated. The current through the biasing network can be of the order of a few tens of nA, and therefore the power consumption of the biasing network is miniscule. At the startup as the output of each rectifier stage increases the bias voltages (V_{osn} and V_{osp}) also increase until the rectifier reaches its desirable operation. This technique has the following advantages: (a) considerably smaller die area compared to the switched-capacitor network since no large capacitor (C_{bias}) is required (b) makes the rectifier self-sufficient. In RFID tags self-sufficient rectifiers are preferable since they do not require any additional components to function, e.g., an additional battery.

IV. POST- LAYOUT AND SCHEMATIC- LEVEL SIMULATION RESULTS

To illustrate the performance improvement of the proposed circuit at low-input RF powers the standard four-stage "four-transistor-cell" rectifier [6, 7] and the proposed four-stage driven-gate rectifier with transistor chain biasing (Fig. 5) are design and laid out in a 0.13 µm CMOS

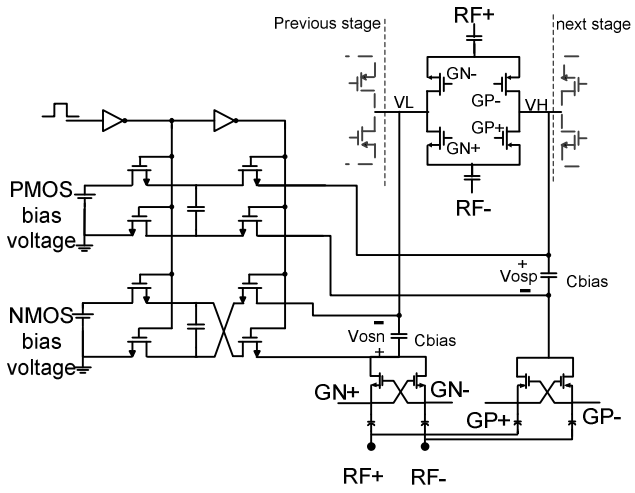


Fig 4. Connection of recharging circuit to one stage of the rectifier

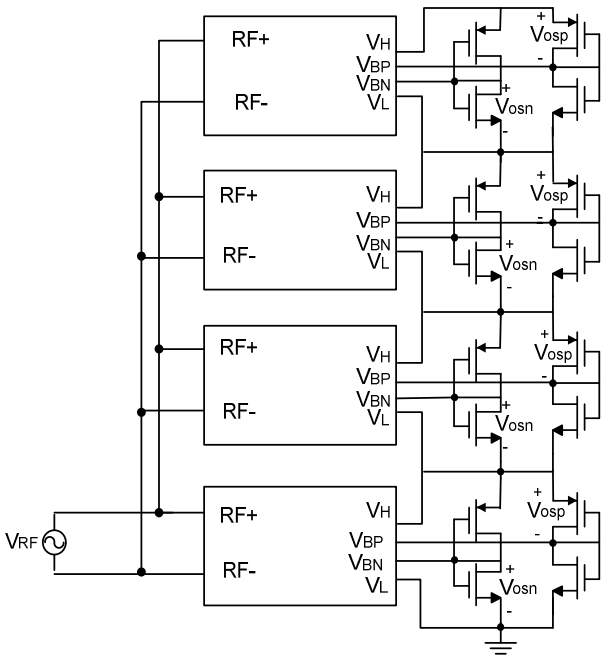
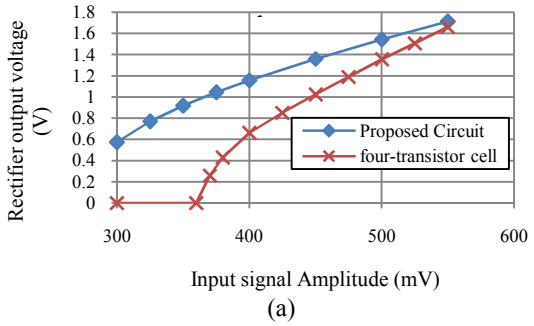


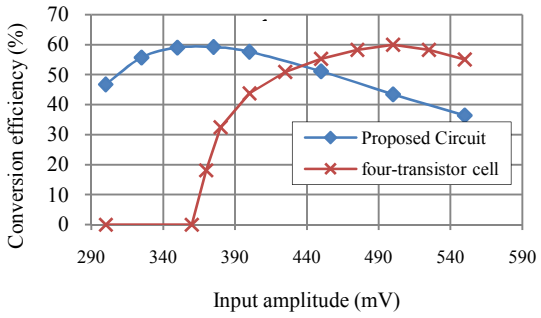
Fig 5. A 4-stage driven-gate rectifier with transistor chain bias

technology. In this section, we present the post-layout simulation results for these two circuits. Both offset voltages (V_{osn} and V_{osp}) are about 150 mV.

The output voltage and the conversion efficiency have been shown in Fig. 6 for different RF input voltage amplitudes at the load current equal to 4 µA. Note that, as can be seen from Figs. 6(a) and 6(b), when the input amplitude increases beyond the value where the efficiency is maximum, the output voltage of the rectifier still increases, however, the PCE drops, that is, the rate of output voltage variation decreases. This is the so-called self-output-power regulation function that is discussed in [7].



(a)



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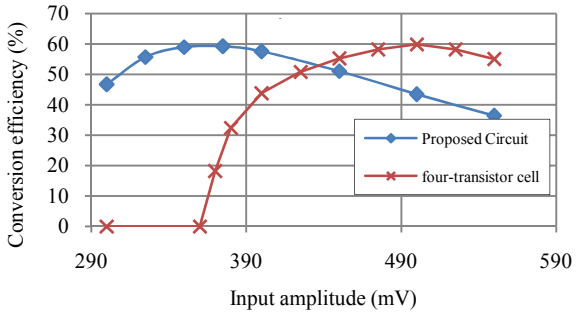
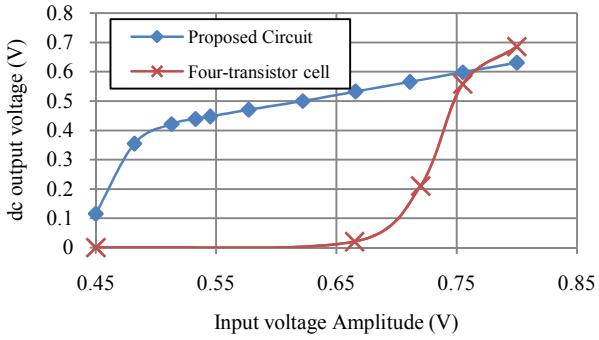
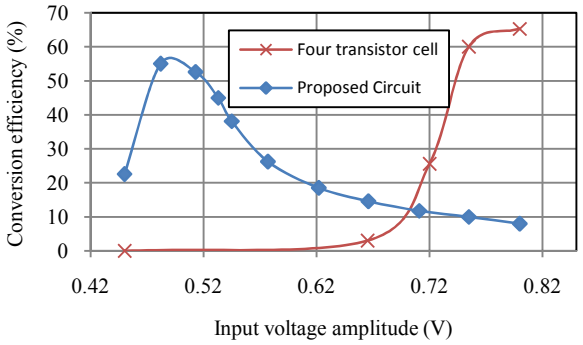


(c)

Fig 6. Performance comparison of rectifiers based on the standard four-transistor cell and proposed "driven-gate" structures designed in 0.13 µm CMOS for a load current of 4 µA (post-layout simulations): (a) rectifiers output voltages (b) efficiency (note that in the proposed structure the peak efficiency is shifted 150 mV to the right, towards lower input RF voltages, as compared to that of the conventional four-transistor cell. (c) efficiency as a function of input power.



(a)



(b)

Fig 7. (a) Rectifiers output voltages (b) Efficiency comparison for 0.35 µm technology.

As it can be seen in Fig. 6(b), the efficiency profile of the driven-gate rectifier is similar to that of four-transistor cell except that it has a 150 mV shift to the right. Increasing the bias voltages will further shift the maximum to the right. Smaller V_{RF} is also required to reach a certain output DC voltage for rectifier output voltage less than 1.65 V. Fig. 6(c) shows that the power that the maximum efficiency happens moves to a lower power in the driven gate rectifier.

Similar simulations (however at the schematic-level and not the post-layout level) have been performed on a standard single-stage four-transistor-cell structure [6, 7] and the proposed driven-gate rectifier in a 0.35 µm CMOS technology with the load current of 1 µA (Fig. 8). Relatively large threshold voltages in 0.35 µm technology, in general makes it unsuitable for low-power operation; however, the simulation results show that using the presented approach low power rectifiers can be implemented in such a technology. For the purpose of comparison, the typical process parameters of 0.13 µm and 0.35 µm CMOS technologies that are used here are given in Table.1.

Table1. Typical CMOS Process Parameter

Parameter	0.35µm	0.13 µm
Minimum MOS length	0.35 µm	0.12 µm
NMOS Vth	0.574V	0.355V
PMOS Vth	-0.716V	-0.325V
V_{DD}	3.3V	1.6V
Gate oxide capacitance	5.89 fF/ µm^2	10.5 fF/ µm^2

Note that the proposed driven-gate rectifier has an acceptable performance (refer to Figs. 6 and 7) even for input RF voltage amplitudes that are smaller than the transistor V_{th}. This is an important property and can be taken advantage of to improve the sensitivity of the rectifier (to reduce the minimum RF input amplitude from which the rectifier can still operate) or to design rectifiers in less-expensive (older generation) technologies in which the V_{th} of transistors is so high that the input RF amplitude is below or barely exceeds that value.

In the simulations presented here, the leakage current through V_B is less that 8 nA in 0.13 µm CMOS and less than 3 nA in 0.35 µm CMOS (excluding the leakage current through the biasing circuit switch transistors).

In the proposed driven-gate rectifier, the capacitors in the drivers can be small and these capacitors only have to be much greater than the parasitic capacitances of the transistors. In the simulations of the driven-gate rectifier in 0.13µm CMOS $C_1 = C_2 = 100\text{fF} - 200\text{fF}$ and $C_r = 1\text{pF}$. Smaller capacitances decrease the required die area of the chip. The layout area is 200 µm × 94 µm. In 0.35 µm $C_1 = C_2 = C_r = 1\text{pF}$.

V. CONCLUSION

A high-efficiency highly sensitive CMOS rectifier is presented that uses custom-designed driver stages. The circuit only uses standard-V_{th} transistors and can operate even when the input RF voltage amplitude is smaller than the transistor V_{th}. At a given RF input power, the drivers keep the DC voltage level of the gate of the rectifier transistors at the optimum level to maximize the efficiency of the rectifier. The bias voltage can be tuned so that the maximum efficiency is achieved for any given input power. The proposed technique is suitable for achieving high efficiency when the rectifier RF input power is weak.

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