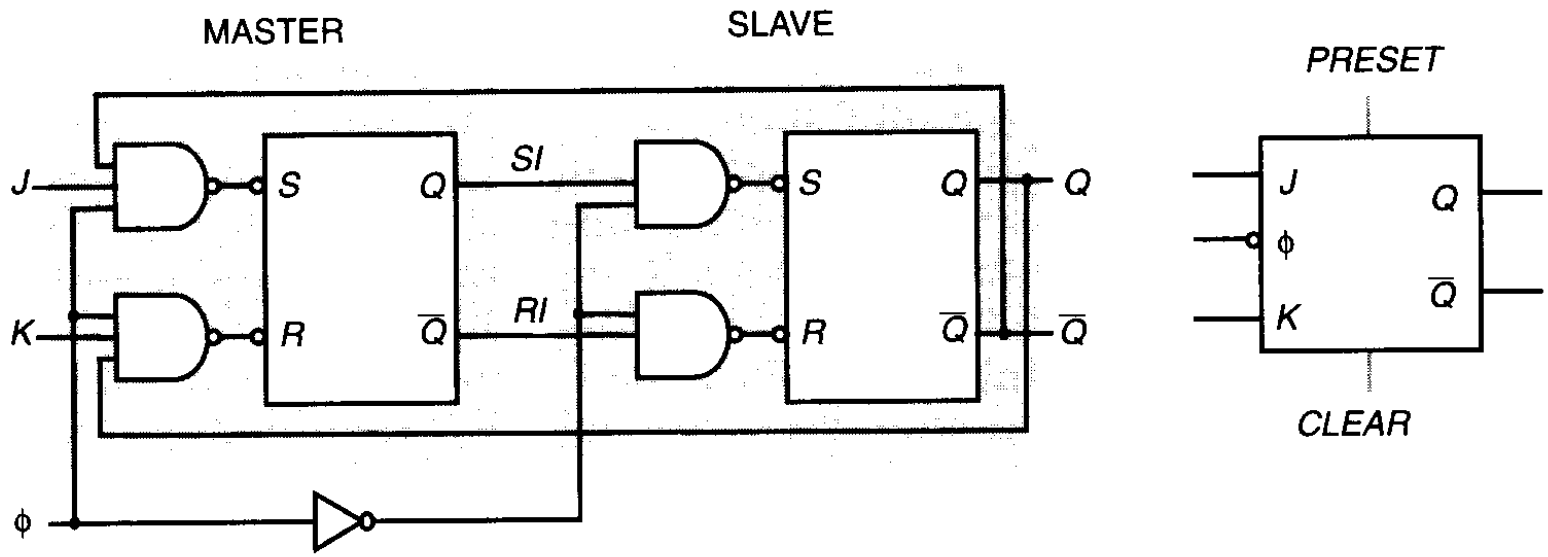
Master-Slave Flip-Flop



- Either master or slave FF is in the hold mode
- Pulse lengths of clock must be longer than propagation delay of latches
- Asynchronous or synchronous inputs to initialize the flip-flop states

One-Catching or Level-Sensitive