THEORY OF OPERATION

DDS CORE

The AD9959 has four DDS cores each consisting of a 32-bit phase accumulator and phase-to-amplitude converter. Together, these digital blocks generate a digital sine wave when the phase accumulator is clocked and the phase increment value (frequency tuning word) is greater than 0. The phase-to-amplitude converter simultaneously translates phase information to amplitude information by a COS (θ) operation.

The output frequency (f_O) of each DDS channel is a function of the rollover rate of each phase accumulator. The exact relationship is given in the following equation:

$$f_O = \frac{(FTW)(f_S)}{2^{32}} \; with \; 0 \le FTW \le 2^{31}$$

where:
f_S = the system clock rate
FTW = the frequency tuning word
2^{32} represents the phase accumulator's capacity.

Since all four channels share a common system clock, they are inherently synchronized.

The DDS core architecture also supports the capability to phase offset the output signal. This is performed by the channel phase offset word (CPOW). The CPOW is a 14-bit register that stores a phase offset value. This value is added to the output of the phase accumulator to offset the current phase of the output signal. Each channel has its own phase offset word register. This feature can be used for placing all channels in a known phase relationship relative to one another. The exact value of phase offset is given by the following equation:

$$\Phi = \left(\frac{POW}{2^{14}} \right) \times 360^\circ$$

D/A CONVERTER

The AD9959 incorporates four, 10-bit current output DACs. The DAC converts a digital code (amplitude) into a discrete analog quantity. The DAC's current outputs can be modeled as a current source with high output impedance (typically 100 kΩ). Unlike many DACs, these current outputs require termination into AVDD via a resistor or a center-tapped transformer for expected current flow.

Each DAC has complementary outputs that provide a combined full-scale output current (I_{OUT} + I_{OUTB}). The outputs always sink current and their sum equals the full-scale current at any point in time. The full-scale current is controlled by means of an external resistor (R_{SET}) and the scalable DAC current control bits discussed in the Modes of Operation section. The resistor R_{SET} is connected between the DAC_RSET pin and analog ground (AGND). The full-scale current is inversely proportional to the resistor value as follows:

$$R_{SET} = \frac{18.91}{I_{OUT}}$$

The maximum full-scale output current of the combined DAC outputs is 15 mA, but limiting the output to 10 mA provides optimal spurious-free dynamic range (SFDR) performance. The DAC output voltage compliance range is AVDD + 0.5 V to AVDD − 0.5 V. Voltages developed beyond this range can cause excessive harmonic distortion. Proper attention should be paid to the load termination to keep the output voltage within its compliance range. Exceeding this range could potentially damage the DAC output circuitry.

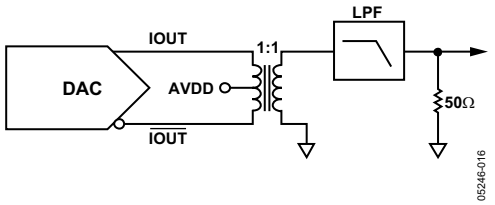

Figure 31. Typical DAC Output Termination Configuration